Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-52 (cancelled)

Claim 53 (previously presented) In a data processing system, a method for ordering a plurality of memory access requests, the method comprising:

accepting the plurality of memory access requests;

ordering the plurality of memory access requests, wherein the plurality of memory requests are ordered based on age and availability of corresponding memory locations; and

after the ordering, servicing the plurality of memory requests.

Claim 54 (previously presented) The method of claim 53 wherein plurality of memory access requests comprises at least three memory access requests.

Claim 55 (cancelled)

Claim 56 (previously presented) In a computer system, a method for processing a plurality of memory access requests, the method comprising:

receiving said plurality of memory access requests by a queue;

reordering said plurality of memory access requests in the queue based on their age and the availability of target memory addresses, wherein a target memory address is associated with a memory access request of the plurality of memory access requests;

after said reordering, servicing said plurality of memory access requests.

Claim 57 (previously presented) The method of claim 56 wherein said reordering provides for at least two memory access requests with available target memory addresses.

Claim 58 (previously presented) The method of claim 56 wherein said servicing is done sequentially.

Claim 59 (previously presented) The method of claim 56 wherein said queue is a priority queue, wherein a first memory access requests with higher priority than a second memory access request is executed before said second memory access request.

Claim 60 (previously presented) The method of claim 56 wherein said reordering results in a queue having a first memory access request with an available target memory address preceding a second memory access request with an unavailable target memory address.

Claim 61 (previously presented) The method of claim 56 further comprising, after said servicing of said plurality of memory access requests, returning results of said servicing according to a received order of said plurality of memory access requests by said queue.

Claim 62 (previously presented) A data processing system that reorders memory access requests, the system comprising:

a request buffer for holding a plurality of memory access requests received in a first order;

an availability determiner for determining availability of memory locations requested by said plurality of memory access requests; and

a reordering unit responsive to said availability determiner for arranging said plurality of memory access requests in a second order based on request ages and the availability of memory locations, wherein a first memory request of said plurality of memory access requests with an available memory location precedes a second memory request of said plurality of memory access requests with an unavailable memory location.

Claim 63 (previously presented) The method of claim 62 further comprising an execution unit for executing said plurality of memory access requests based on said second order.

Claim 64 (previously presented) A priority queue in a computer system for determining an execution order for executing a plurality of memory access requests, the priority queue comprising:

a memory unit for storing said plurality of memory access requests in a receiving order; and

an ordering module for determining said execution order from said receiving order, said execution order is based on availability of target memory addresses associated with said plurality of memory access requests as well as an initial priority of the request, the initial priority determined by identities of memory access request sources.

Claim 65 (previously presented) The method of claim 64 wherein said plurality of memory access requests comprises at least three memory access requests.

Claim 66 (previously presented) The method of claim 64 further comprising an execution unit for executing said plurality of memory access requests in said execution order.

Claim 67 (previously presented) The method of claim 66 further comprising a results ordering module for returning results of said execution unit according to said receiving order.

Claim 68 (previously presented) In a data processing system, a method for ordering a plurality of memory access requests, the method comprising:

accepting the plurality of memory access requests;

ordering the plurality of memory access requests, wherein the plurality of memory requests are ordered based on an initial priority and availability of a corresponding memory location, the initial priority determined by identities of memory access request sources, and wherein a first request of the plurality of memory access requests to a first memory bank that is

not currently being accessed precedes a second request of the plurality of memory access requests to a second memory bank that is currently being accessed; and

after the ordering, servicing the first request.

Claim 69 (previously presented) In a computer system, a method for processing a plurality of memory access requests, the method comprising:

receiving said plurality of memory access requests;

reordering said plurality of memory access requests based on request age and the availability of target memory addresses, wherein a target memory address is associated with a memory access request of the plurality of memory access requests and a target memory address is available if it is located in a memory bank that is not currently being accessed;

after said reordering, servicing said plurality of memory access requests.

Claim 70 (previously presented) The method of claim 69 wherein said servicing is done sequentially.